Attorney Docket No. 9180-24 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re: Rinne
Application No.: 10/689,976
Filed: October 21, 2003
For: STACKED ELECTRONIC STRUCTURES INCLUDING OFFSET SUBSTRATES

U.S. Patent No.: 7,495,326 B2
Issued: February 24, 2009
Confirmation No: 3798

March 27, 2009

Commissioner for Patents
Attn: Certificate of Correction Branch
P.O. Box 1450
Alexandria, VA 22313-1450

REQUEST FOR ENTRY OF CERTIFICATE OF CORRECTION UNDER No. 35 U.S.C §254 AND 37 C.F.R. §1.322

Sir:

The Assignee of record for the above-referenced patent hereby requests, pursuant to 35 U.S.C §254 and 37 C.F.R. §1.322, that a Certificate of Correction be issued. This request is made in order to correct the mistakes incurred through the fault of the U.S. Patent and Trademark Office. The mistakes appearing in the patent are set forth with corrections on the Certificate of Correction enclosed herewith. The Assignee further directs the Commissioner's attention to the attached Amendment filed March 6, 2006, requesting the insertion, not replacement of, the noted paragraph.

No fee is believed due. However, the Commissioner is authorized to charge any deficiency or credit any overpayment to Deposit Account No. 50-0220.

Respectfully submitted,

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CERTIFICATION OF ELECTRONIC TRANSMISSION

I hereby certify that this correspondence is being transmitted via the Office electronic filing system in accordance with § 1.6(a)(4) to the U.S. Patent and Trademark Office on March 27, 2009.

Jessica M. French

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 7,495,326 B2

APPLICATION NO.: 10/689,976

ISSUE DATE: February 24, 2009

INVENTOR(S) : Rinne

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 9, Line 30: Please insert the following paragraph:

-- As shown in the cross section of Figure 5, a stack of substrates **10a-c** may be mounted on a substrate **210** (such as a printed circuit board PCB) on which conductors have been provided corresponding to the small solder bumps **40**, the conductive traces **30**, and the large solder bumps **50**. A signal path **60**, for example, may be provided from the substrate **210** through large bump **50a** into conductive trace **30a** along the device side of the substrate **10a** to small bump **40a**, and then down to a small pad **240** on the substrate **210** below, then across the face of the substrate **210** and up through the large bump **50b** of the second substrate **50b**. The signal may then traverse the device side (active face) of the second substrate **10b** through conductive trace **30b** and down through small bump **40b** into the small pad **140a** on the backside (inactive face) of the first substrate **10a**, and then through conductive trace **130a** to the large pad **150a** and up through the large bump **50c** of the third substrate **10c**. This zig-zag interconnection topology may continues up through a stack of any number of substrates **10**. --

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

Column 16, Claim 15, Line 8: Please correct "claim 13" to read -- claim 14 --

Column 20, Claim 36, Line 10: Please correct "claim 34" to read -- claim 35 --

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Attorney Docket No. 9180-24 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re: Glenn A. Rinne; Conf. No. 3798
Application No.: 10/689,976 Group Art Unit: 2811
Filed: October 21, 2003 Examiner: Jennifer E. Matisiak
For: **STACKED ELECTRONIC STRUCTURES INCLUDING OFFSET SUBSTRATES**

Date: March 6, 2006

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT

Sir:

Applicants provide the present Amendment to address the issues raised in the Office Action mailed December 29, 2005.

It is not believed that an extension of time and/or additional fee(s)-including fees for net addition of claims-are required, beyond those that may otherwise be provided for in documents accompanying this paper. In the event, however, that an extension of time is necessary to allow consideration of this paper, such an extension is hereby petitioned under 37 C.F.R. §1.136(a). Any additional fees believed to be due in connection with this paper may be charged to our Deposit Account No. 50-0220.

Amendments to the Specification are provided on page 2 of this paper.

Amendments to the Claims are reflected in the listing of claims, which begins on page 3 of this paper.

Remarks begin on page 19 of this paper.

In The Specification:

At page 14, after line 11, please insert the following paragraph:

As shown in Figures 2a-b, the substrate **10** may have opposing first and second surfaces (*e.g.* the device side **20** and backside **120**). The solder bumps **40** may provide a first array of interconnection structures on the device side **20** of the substrate **10**, and the first array of interconnection structures may be arranged in a first pattern. The contact pads **140** may provide a second array of interconnection structures on the backside **120** of the substrate **10**, and the second array of interconnection structures may be arranged in a second pattern and that is a mirror image of the first pattern. The solder bumps **50** may provide a third array of interconnection structures on the device side **20** of the substrate **10** spaced apart from the first array of interconnection structures, and the third array of interconnection structures may be arranged in a third pattern. The contact pads **150** may provide a fourth array of interconnection structures on the backside **120** of the substrate **10** spaced apart from the second array of interconnection structures, and the fourth array of interconnection structures may be arranged in a fourth pattern that is a mirror image of the third pattern.